## REMARKS

The courtesy of Examiner Gerstl in granting the interview of March 22, 2005, is acknowledged with appreciation. The following amendment amends the Title of the Application and the Claims. Claims 1, 4, 5, 9, 10, 11, 21, 29, 32, 33, and 49 are amended, and new Claim 50 is added. No new matter and no new issues are raised by these amendments. Support for new Claim 50 can be found on page 13, lines 8-10, Figure 2, and through out the remainder of the specification. Now in the application are Claims 1-50 of which Claims 1, 21, 22, 28, 29, and 49 are independent. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

## OBJECTION TO SPECIFICATION

The title of the invention stands objected to as non-descriptive. In response, Applicants amend the title in the forgoing amendment to add further descriptive language as requested by the Examiner. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the objection to the specification.

## CLAIM OBJECTIONS

Claims 5-17, 19-20, 34-45, 47, and 48 stand objected to for improper dependent form. MPEP §608.01(n) is cited in support of the objection. Nevertheless, Applicants respectfully choose to defer the renumbering of the Claims until allowable subject matter is identified to avoid further confusion during prosecution. Accordingly, Applicants respectfully request the Examiner to continue the objection under MPEP §608.01(n) until an indication of allowable subject matter.

## CLAIM REJECTIONS UNDER 35 U.S.C. §102

The Office Action rejects Claims 1-49 as being anticipated by U.S. Patent No. 5,758,112 of Yeager, *et al.*, (hereinafter "Yeager"). Applicants respectfully traverse this rejection on the basis of the above amendments and the following arguments, and further contend that Yeager fails to

disclose all elements of these amended claims, as described below, and hence, does not anticipate the claimed inventions.

For purposes of clarity in the discussion below, the respective claim rejections under 35 U.S.C. §102 are discussed separately.

A. Rejection of Claims 1-20 under 35 U.S.C. §102(b):

The Office Action rejects Claims 1-20 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the amendment to Claim 1 above and the following arguments, and further contend that Yeager fails to disclose all elements of these claims, as amended, and hence does not anticipate the claimed invention. Specifically, Applicants assert Yeager does not disclose a set of pointers that includes at least two pointers set apart by a fixed distance and move in unison, at all times, up and down a structure.

Claims 2-20 depend directly or indirectly upon amended Claim 1 and thereby incorporate the patentable features of amended Claim 1.

Amended Claim 1 is directed to a method performed in a microprocessor performing speculative instruction execution. The method includes a step of providing a structure to track register allocation for a first thread of the microprocessor. The method also includes a step of tracking a first set of pointers in the structure designed to manage the register allocation for an instruction of the first thread of the microprocessor to prevent a register allocated as a destination operand for the instruction from being overwritten before the instruction retires. The first set of pointers includes at least two pointers set apart by a fixed distance that move in unison, at all times, up and down the structure.

An advantage of the method of the present invention is the ability to perform an instruction pipeline flush without having to physically restore register values.

The Yeager patent is directed to a method and apparatus for storing register renaming information in the event of a branch misprediction. Yeager discloses redundant mapping tables for use in microprocessors that rename registers and perform branch prediction. The redundant mapping tables include a number of primary RAM cells coupled to a number of redundant RAM cells. In the event of a branch instruction, the redundant RAM cells can save the contents of the primary RAM cells in a single clock cycle before the microprocessor decodes and executes subsequent instructions along a predicted branch path. Should the branch instruction be mispredicted, the redundant RAM cells can restore the primary RAM cells in a single clock cycle. To accomplish this, Yeager discloses a free register list coupled to a mapping table, which in turn is coupled to an instruction queue and the instruction queue is coupled to a register file. The free register lists disclosed by Yeager each include a read pointer and write pointer to identify entries in selected RAMs. Yeager moves the write pointer in increments determined by the member of instructions which graduate during each clock cycle. Likewise, Yeager moves the read pointer in increments by the number of free registers assigned during each clock cycle. The Yeager patent does not anticipate amended Claim 1.

The Yeager patent discloses two separate structures for tracking register allocation for instructions. Each such structure disclosed by Yeager includes two pointers, a read pointer and a write pointer that operate independent of each other. In contrast, amended Claim 1 recites a step of tracking in a structure a set of pointers that includes at least two pointers set apart by a fixed distance and move in unison, at all times, up and down the structure. The Yeager patent does not disclose two pointers set apart by a fixed distance that move in unison, at all times, up and down a structure to track register allocation of a first thread of a microprocessor. In fact, the Yeager patent discloses that the read pointer of the free list is incremented by the number of free registers assigned during each cycle. While the write pointer is incremented by the number of instructions with graduate during each cycle. Hence, the read pointer and the write pointer in each structure disclosed by Yeager do not move in unison, but rather independently.

Yeager fails to anticipate amended Claim 1 and hence, fails to anticipate Claims 2-20, which depend directly or indirectly upon amended Claim 1. Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claims 1-20 under 35 U.S.C. §102(b).

B. Rejection of Claim 21 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 21 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of this claim as described below, and hence, does not anticipate the claimed invention. Specifically, Applicants assert Yeager does not disclose a single structure to track register allocation for a first thread and a second thread of a multithreading microprocessor.

Amended Claim 21 is directed to a method performed in a multithreading processor performing speculative instruction execution. Performance of the method provides a single structure to track register allocation for a first thread and a second thread of the multithreading microprocessor. The method includes a step of tracking a first set of pointers in the structure assigned to manage register allocation of an instruction of the first thread of the multithreading processor and includes a step of tracking a second set of pointers in the structure assigned to manage the register allocation of an instruction of the second thread of the multithreading processor. Amended Claim 21 is not anticipated by Yeager, because Yeager does not disclose a single structure to track register allocation for a first and second thread of a multi-threading processor.

The Yeager patent discloses two independent free register lists for managing register allocation. Specifically, free register list (208) manages registers associated with floating point instructions and free register list (210) manages registers associated with integer related instructions. Nowhere does Yeager disclose that the floating point free register list and the integer free register list are a single structure. In contrast, amended Claim 21 recites a step of providing a single structure to track register allocation for a first thread and a second thread of the multithreading processor. Performance of the method recited in amended Claim 21 tracks at least two sets of pointers in the provided structure. Nowhere does Yeager disclose the tracking of two sets of

pointers in a single structure. Yeager tracks one set of pointers in a first structure and a second set of pointers in a second structure. Accordingly, the microprocessor disclosed by the Yeager patent has an architecture, operation and function different from the architecture, function and operation of the method performed in a multithreading microprocessor performing speculative instruction execution recited in amended Claim 21.

Applicants note the original language of Claim 21 is clear and distinct leading to one and only one correct interpretation in contrast to the interpretation adopted by the Examiner. Moreover, Applicants assert the record in the instant application is free of remarks contending the Examiner can validly view elements 204, 206, 208, and 210 of Yeager to be a single structure with two parts, one for a floating point thread and another for an integer thread. If the Examiner wishes to maintain this assertion, Applicants respectfully request the Examiner to cite such passages from the record in support of his assertion. Nonetheless, to assist in expediting prosecution, Applicants amend Claim 21 to recite a single structure, although proper grammatical interpretation of the original claim language provides no other reasonable interpretation.

Contrary to the assertion in paragraph 61 of the Final Office Action mailed November 16, 2004, nothing in *In re Larson*, 340 F.2d 965, 144 USPQ 347 (CCPA 1965) supports a conclusion that the single structure of Claim 21 is merely an engineering choice and not patentable. A careful reading of *In re Larson* concerns a mechanical assembly, which in the prior art included several parts rigidly secured together as a single unit versus the recitation in U.S. patent application serial No. 7282 of a like assembly having a unitary construction. The Court held the prior art assembly comprising several parts rigidly secured together as a single unit were so combined as to constitute a unitary whole and hence the use of a one-piece construction versus the multiple-piece construction of the mechanical assembly was a matter of engineering design choice. No such replication of an assembly so combined with fasteners and later formed without fasteners is recited in Claim 21. That is, the two structures disclosed by Yeager are separate, distinct, and not so combined to constitute a unitary whole structure.

Clearly, as processors have become larger and more complicated, internal data and program storage in the form of register files and cache arrays consume an increasing portion of the transistor count and die area. Consequently performance, power, yield, and reliability of the overall die is greatly influenced by the design of the structured holding physical registers and the design of structures used to track register allocation for multiple threads of the processor. Speculative processors utilize a load store architecture that typically requires a large number of general purpose registers. Performance boost innovations such as register renaming and register windowing further expand the number of general purpose registers. Typically, the general purpose register arrays are located inside the data paths of execution units. Consequently, the register file layout must occur on the same pitch as the data path. Because the data path pitch is wider than a typical SRAM cell, the register can use devices that are larger than typically used in large SRAM design. Thus, some of the issues typically associated with SRAM design are reduced. The Yeager patent teaches such an architecture by placing register files 302 and 306 inside the data path of respective execution units.

Consequently, the architecture, function, and operation of a superscalar processor as disclosed by Yeager having two separate and distinct caches of general purpose registers to facilitate operational performance teaches that each register array requires in close proximity thereto a dedicated structure for managing free registers. Hence, Yeager discloses a floating point free register list 208 separate and distinct from the integer free register list 210.

Contrary to the Examiner's assertions, one skilled in the art would not be motivated to combine the two free register lists into a single structure as Applicants have claimed in amended Claim 21. Those skilled in the art along with the prior art teach placement of separate and distinct dedicated structures for managing registers in close proximity to respective array structures to facilitate association of physical registers with logical registers and hence facilitate operational performance of a superscalar processor. Hence, the use of a single structure to track registers for two threads of a superscalar processor results in a change in structure, function and operation that is patentable and not merely engineering choice.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 21 under 35 U.S.C. §102(b).

C. Rejection of Claims 22-27 Under 35 U.S.C. §102(b):

The Office Action rejects Claims 22-27 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of these claims, and hence, does not anticipate the claimed invention. Specifically, Applicants assert Yeager does not disclose a retire row pointer.

Claims 21-27 depend, directly or indirectly upon Claim 22 and therefore incorporate the patentable features of Claim 22.

Claim 22 is directed to a semiconductor device having a number of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out of order execution. The semiconductor device includes a first module providing a structure for holding information identifying available physical registers for the microprocessor and a first set of register pointers assigned to a first portion of the structure. The first set of register pointers track the physical registers assigned as destination registers for a first thread of the microprocessor. The first set of register pointers includes a retire row pointer to identify where a pointer pointing to at least one of the physical registers assigned as a destination register for an instruction in the first thread that is next to be retired. The Yeager patent does not anticipate Claim 22 because Yeager fails to disclose a retire row pointer.

Yeager discloses a read pointer and a write pointer, however, Yeager does not disclose a retire pointer. The Yeager patent discloses a graduation mask used to identify which instruction graduated. A mask is not a pointer. A mask is a binary value used to selectively screen out or let through certain bits and a value. In contrast, a pointer is a variable that contains the address of a storage location.

In the Office Action a dictionary definition of "pointer" is relied upon in support that a mask and a pointer are the same. The cited definition of "pointer" reads "an identifier that indicates the location of an item of data". Applicants do not disagree with this definition, but further elaborate on the definition. That is, the location of an item of data refers to a memory location (address) of some data rather than the data itself. Contrary to the provided definition of a "pointer", the Microsoft Computer Dictionary, 4th Ed., defines a "mask" as "a binary value used to selectively screen out or let through certain bits in a data value. Masking is performed by using a logical operator to combine the mask and the data value." Hence, one skilled in the art would clearly recognize that a mask and a pointer have distinct uses, operations and functions and therefore have a patentable distinction.

The Yeager patent supports the patentable distinction between a "pointer" and a "mask". The Yeager patent discloses when an instruction graduates, the "old" physical register number associated with its destination register is written back into the appropriate free register list. To write each number into the correct RAM, each write port includes a four input MUX which can select from any of the four graduating instructions. The controls for these multiplexers depend on graduation mask (850), ActIntDest (852), and the two low bits of the write pointer. The mask, which (together with signal 852) indicates which of the four graduating instructions is releasing an integer register is decoded into four two-bit signal pairs. Hence, the graduation mask, in combination with signal 852 and a selected multiplexer, operates as an address decoder to create a memory address. *See*, 14, lines 32 through 46 of Yeager. By contrast, a pointer contains the decoded address and is not used to create the address. Accordingly, Applicants respectfully contend that the semiconductor device of Claim 22 is patentably distinct from the semiconductor device disclosed by Yeager.

As such, the Yeager patent discloses a semiconductor device having a structure, operation and function, different from the structure, operation and function of the semiconductor device recited in Claim 22. Accordingly, Yeager does not anticipate Claim 22 or dependent Claims 23-27.

Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 22-27 under 35 U.S.C. §102(b).

D. Rejection of Claim 28 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 28 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that Yeager fails to disclose all elements of this claim, as described below, and hence, does not anticipate the claimed invention. Applicants assert Yeager does not disclose a partitionable structure as recited in Claim 28.

Claim 28 is directed to a semiconductor device having a number of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out of order execution. The semiconductor device includes a first module providing a structure for holding information identifying available physical registers of the microprocessor, a first set of register pointers assigned to a first portion of the structure and a second set of registers assigned to a second portion of the structure. The Yeager patent does not anticipate Claim 28.

The Yeager patent discloses a first structure for holding information identifying available physical registers in a floating point instruction pipeline and a second structure for identifying available physical registers and a second pipeline or integer instruction pipeline of the microprocessor. In contrast, the semiconductor device of Claim 28 discloses a structure partitionable to hold at least two sets of register pointers to track the assignment of destination registers for at least two threads of a microprocessor performing out of order execution. Nowhere does the Yeager patent disclose a partitionable structure to track physical register assignments corresponding to either two threads or two instruction pipelines of a microprocessor. The Yeager patent discloses a single structure for each thread or instruction pipeline that includes a set of register pointers assigned to track physical registers assigned as destination registers for instructions in each respective thread or instruction pipeline. Accordingly, the semiconductor device of the Yeager patent has an architecture and a structure along with a function and an operation different

from the architecture, structure, function, and operation of the semiconductor device of Claim 28. Hence, the Yeager patent does not anticipate Claim 28. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 28 under 35 U.S.C. §102(b).

E. Rejection of Claims 29-48 under 35 U.S.C. §102(b):

The Office Action rejects Claims 29-48 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the amendment to Claim 29 above and the following arguments, and further contend that Yeager fails to disclose all elements of these claims, as amended, and hence does not anticipate the claimed invention. Applicants assert Yeager does not disclose a set of pointers that includes at least two pointers set apart by a fixed distance and move in unison, at all times, up and down a structure.

Claims 30-48 depend directly or indirectly upon amended Claim 29 and thereby incorporate the patentable features of amended Claim 29.

Amended Claim 29 is directed to a computer readable medium holding computer executable instructions for performing a method in a microprocessor performing speculative instruction execution. The method includes a step of providing a structure to track register allocation for a first thread of the microprocessor. The method also includes a step of tracking a first set of pointers in the structure designed to manage the register allocation for an instruction of the first thread of the microprocessor to prevent a register allocated as a destination operand for the instruction from being overwritten before the instruction retires. The first set of pointers includes a first pointer and a second pointer set apart by a fixed distance that move in unison, at all times, up and down the structure.

The Yeager patent discloses two separate structures for tracking register allocation for instructions. Each such structure disclosed by Yeager includes two pointers, a read pointer and a write pointer that operate independent of each other. In contrast, amended Claim 29 recites a step of tracking in a structure a set of pointers that includes a first pointer and a second pointer set apart by

a fixed distance and move in unison, at all times, up and down the structure. The Yeager patent does not disclose two pointers set apart by a fixed distance that move in unison, at all times, up and down a structure to track register allocation of a first thread of a microprocessor. In fact, the Yeager patent discloses that the read pointer of the free list is incremented by the number of free registers assigned during each cycle. While the write pointer is incremented by the number of instructions with graduate during each cycle. Hence, the read pointer and the write pointer in each structure disclosed by Yeager do not move in unison, but rather independently.

Yeager fails to anticipate amended Claim 29 and hence, fails to anticipate Claims 30-48, which depend directly or indirectly upon amended Claim 29. Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claims 29-48 under 35 U.S.C. §102(b).

F. Rejection of Claim 49 Under 35 U.S.C. §102(b):

The Office Action rejects Claim 49 as being anticipated by Yeager. Applicants respectfully traverse this rejection on the basis of the above amendments and the following arguments, and further contend that Yeager fails to disclose all elements of this amended claim as described below, and hence, does not anticipate the claimed invention. Specifically, Applicants assert Yeager does not disclose a single structure to track register allocation for a first thread and a second thread.

Amended Claim 49 is directed to a computer readable medium holding computer executable instructions for performing a method in a multithreading processor performing speculative instruction execution. Performance of the method provides a single structure to track register allocation for a first thread and a second thread of the multithreading microprocessor. The method includes a step of tracking a first set of pointers in the structure assigned to manage register allocation of an instruction of the first thread of the multithreading processor and includes a step of tracking a second set of pointers in the structure assigned to manage the register allocation of an instruction of the second thread of the multithreading processor. Amended Claim 49 is not anticipated by Yeager.

The Yeager patent discloses two independent free register lists for managing register allocation. Specifically, free register list (208) manages registers associated with floating point instructions and free register list (210) manages registers associated with integer related instructions. Nowhere does Yeager disclose that the floating point free register list and the integer free register list are a single structure. In contrast, amended Claim 49 recites a step of providing a single structure to track register allocation for a first thread and a second thread of the multithreading processor. Performance of the method recited in amended Claim 49 tracks at least two sets of pointers in the provided structure. As discussed in connection with the rejection of Claim 21, nowhere does Yeager disclose the tracking of two sets of pointers in a single structure. Yeager tracks one set of pointers in a first structure and a second set of pointers in a second structure. Accordingly, the microprocessor disclosed by the Yeager patent has an architecture, operation, and function different from the architecture, function, and operation of the method performed in a multithreading microprocessor performing speculative instruction execution recited in amended Claim 49.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of amended Claim 49 under 35 U.S.C. §102(b).

## NEW CLAIM

New Claim 50 depends from independent Claim 21 and therefore is patentable for at least the reasons discussed above in connection with the rejection of Claim 21 in view of Yeager. Nonetheless, the further recitation in new Claim 50, that the single structure includes at least one protected register region identifying physical register pointers allocated to instructions having a logical destination register decoded and issued but not yet retired, provides a separate further basis for patentability. New Claim 50 is not anticipated by, nor is it rendered obvious by the cited references, either alone or in combination. Accordingly, new Claim 50 is patentably distinct from each of the cited references, either alone or in combination.

## CONCLUSION

In view of the remarks set forth above, Applicants believe that the present invention is in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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